CYBER 960 Computer Systems

CONTROL DATA

Air-cooled mid-range systems for high-performance computing

Mid-range, general-purpose mainframes, the air-cooled CYBER 960 models utilize the most advanced ECL chip technology available.

Control Data CYBER 960 Series computer systems are the mid-range, general-purpose systems that are part of the high-performance CYBER 900 family. These models are part of a binary compatible family that includes the CYBER 930 and CYBER 990 Series. The CYBER 960 provides an upward compatible growth path from CYBER 170 and 180 mainframe systems.

Outstanding performance in multiprogramming environments is the result of the inherent design of the CYBER 960 hardware. The high-performance central processing units (CPUs), coupled with large real memories and high bandwidth input/output units (IOUs), provide ideal platforms for a wide range of applications that require concurrent interactive and batch processing capabilities.

There are three CYBER 960 models—the CYBER 960-11 and CYBER 960-31 are single CPU models, and the CYBER 960-32 is a tightly coupled dual CPU model.

Designed for high-performance in multiprogramming environments, these mid-range models provide:

- One or two CPUs that deliver a general-purpose, large-scale computing capability, offering a performance range from 4 to 13 times the performance of the CYBER 932-11, the new CYBER 900 family entry system.
- Ambient air-cooling system.
- 64-bit word based on eight 8-bit (ASCII) bytes.
- Large real memory ranging from a minimum of 64 million bytes to a maximum of 256 million bytes.
- One or two independent IOUs that offload I/O operations from the CPUs and provide powerful/flexible I/O channel configurations of up to 52 channels with both IOUs. I/O channel data transfer capability ranges from 3 MBytes per second to 15 MBytes per second.
- State-of-the-art circuit technology employing high-speed ECL 200 gate and ECL 6300 gate arrays for logic and 1-MBit dynamic random access memory (DRAM) arrays.
- Highly reliable mainframe hardware produced by a state-of-the-art factory employing the latest manufacturing techniques in automation and robotics.
- Horizontal expansion techniques for system clustering via a high-speed memory link.
- Operation under control of the Network Operating System (NOS) and/or Network Operating System/Virtual Environment (NOS/VE).
- Compact packing in a mainframe complex that includes power cabinet, one or two CPUs, 64 to 256 MBytes of central memory, one I/O unit and the full air-cooled package, and occupies only 26 square feet of floor space.
- Adherence to current industry standards for environmental and safety, including UL, FCC, CSA, IEC, and VDE.

The CYBER 960 models utilize the same basic hardware design to provide three levels of central processing power. These computer systems can be matched to your present computing needs and can be easily adaptable to future requirements. Investments in supporting hardware, peripherals, communications gear, terminal, software, and applications are all protected by the compatibility offered by these three models as well as the entire CYBER 900 mainframe family.

The CYBER 960 computers consist of three basic functions: the central processor, the central memory, and the input/output unit. The following sections provide a brief overview of each function.

Central Processor

A CYBER 960 system includes one or two independent central processors. The CYBER 960-11 and the CYBER 960-31 are single CPU models, and the CYBER 960-32 is a tightly coupled dual CPU model. (Only one CPU can be used when computing under NOS.) Progressive performance upgrades are available for easy field installation.

The following table provides the upgrades available and the relative performance gain.

Model	Relative Performance
960-11	1.0
960-31	1.67
960-32	3.0

Additional floor space is not necessary, as upgrade options to higher performance models are accomplished within existing cabinet space.

Each central processor is an independent micro-coded CPU that features an 11-nanosecond basic clock, a 64-bit word size, a full instruction set including integer, single/double precision floating point, decimal, and byte manipulation instructions as standard. A 32-KByte cache for instruction and data and specialized hardware functional units are utilized to increase performance. A five-stage pipeline holds multiple instructions and addresses during CPU operation. Instructions are issued in a serial manner, but with the pipeline architecture several instructions can be in various stages of execution simultaneously. Controlstore for the micro-code consists of 64 KBytes.

Central Memory

All CYBER 960 systems include a minimum memory size of 64 MBytes with field-installable options to expand it to 128 MBytes, 192 MBytes, or 256 MBytes (maximum). The memory design utilizes a 1-MBit DRAM array. The memory is divided into 8 banks with a data word length of 64 bits plus 8 bits utilized in the single error correction/double error detection (SECDED) circuitry. In addition to the use of SECDED on all stored data, parity protection is designed into all address paths. Memory access time is 308 nanoseconds and each individual bank has a read/write cycle time of 330 nanoseconds. All banks are phased so that successive addresses are to different banks, which increases overall memory performance. The memory bandwidth is an average of one 64-bit word every 44 nanoseconds, or 180 MBytes per second.

The memory is designed to accommodate two independent CPU ports and two independent IOU ports. A data distributor provides service to each of these ports on a priority basis and distributes data between the ports and memory.

Input/Output Unit

CYBER 960 Series systems use one or two separate, independent input/output units (IOU) to perform I/O functions completely separate and independent from the central processors.

The first IOU consists of 20 CYBER peripheral processors (PPs) and 24 3-MBytes per second CYBER 170 I/O channels. The peripheral processors are computational units specifically designed to handle I/O processing. Each of the PPs is an independent unit operating on a 250-nanosecond cycle time and containing 16 KBytes of SECDED protected memory. Each of the 20 PPs has equal access to central memory and all 24 I/O channels. Each of the 24 CYBER 170 I/O channels is a 12-bit plus parity independent, bidirectional data channel with a maximum transfer rate of 3 MBytes per second. Each channel is capable of connecting to as many as eight peripheral controllers.

The IOU also features the optional addition of very high performance I/O processors and I/O channels with direct memory access (DMA). Two options are available with each option adding five I/O processors and five I/O channel interfaces to the basic IOU.

The I/O processors are functionally similar to the initial 20 peripheral processors with additional capability to control DMA I/O channels. Each features independent operation, a 250-nanosecond clock cycle time, and 16 KBytes of SECDED protected memory.

The I/O processors are grouped in two clusters of five each. Each cluster also includes five DMA I/O channel interfaces. I/O channels are only accessible by I/O processors within its cluster. The DMA I/O channels are high-performance 16-bit bidirectional and support the streaming of data directly between peripherals and central memory at data rates up to 16 MBytes per second.

The I/O channel interface design allows a high degree of flexibility in the choice of external channels provided. There are three types of external channels available:

- 19403-21—ISI/DMA Channel rated at 12 MBytes per second.
- 19403-22—170/DMA Channel rated at 15 MBytes per second.
- 19403-23—IPI/DMA Channel rated at 10 MBytes per second, which conforms to the ANSI/FIPS standard for Intelligent Peripheral Interface.

Any combination of the available external channel types is supported. Specific choice of channel types is determined by the channel interface requirements of the selected peripheral equipment.

The IOU utilizes one of the peripheral processors as a maintenance control unit that has access through a special radial interface to the maintenance registers of the central processors, IOUs, and memory. The maintenance control unit in conjunction with the operator console provides the capabilities to initialize the system, monitor operation of the system, verify system integrity through on-line diagnostics, detect system (hardware or software) faults, and initiate corrective action.

Other functions available through the IOU are:

- Free running real-time clock
- Time of day and calendar clock with battery backup
- Reserve communications port for providing Remote Technical Assistance (RTA) by either hardware or software specialists that can be utilized for normal and/or corrective maintenance

Secondary Input/Output Unit

The secondary IOU capability in a CYBER 960 system utilizes the 19403-14 option. This adds a second IOU that contains a base configuration of 10 DMA I/O processors and eight external DMA I/O channels. The DMA I/O processors and DMA I/O channels are identical to the DMA I/O processors and DMA I/O channels offered to expand the base IOU. This secondary IOU can also be expanded in two increments of five DMA I/O processors and five DMA I/O channels. A fully expanded CYBER 960 with all options exercised provides 20 peripheral processors, 24 CYBER 170 3-MBytes per second channels, 30 DMA I/O processors, and 28 DMA I/O channels each with a performance ranging from 10 MBytes per second to 15 MBytes per second.

Operating Environment

CYBER 960 systems are capable of simultaneously executing two different instruction sets (180 state and 170 state) in the same memory and central processor unit.

The 180 state executes the NOS/VE operating system, its products, utilities and applications. This operating environment supports virtual memory addressing, and uses 64-bit words (8-bit bytes) and a 16-bit mode for peripheral processors.

The 170 state executes the NOS operating system, its products, utilities and applications. This operating environment supports real memory addressing, and uses 60-bit words (6-bit characters) and a 12-bit mode for peripheral processors.

The central processor can change states dynamically, running both NOS/VE and NOS at the same time. Central memory and the IOU are divided between the two states at system initialization time, enabling peripheral processors to be assigned to a state.

This unique architecture offers important advantages. Existing NOS users can continue to run their applications on CYBER 960 systems without conversion and without learning a new operating system. Migration is easy and can occur when desired. At the same time, both new and existing users can take advantage of the ease-of-use, power, flexibility, and expandability of the virtual environment provided by NOS/VE.

Ancillary Equipment

The CYBER 960 Series systems are cooled by utilizing computer room ambient air, so there is no requirement for special water cooling equipment.

The systems utilize highly reliable and stable 400 HZ power supplies, which require a 50 HZ or 60 HZ to 400 HZ motor generator.

The 19003-1 Operator Console is required for system initialization as well as for normal operation and diagnostic purposes.

Specifications*

Central Processor

Number of Operating Registers	33
Word Size	64 bits
Clock Cycle Time	11 nsec
Float Point Arithmetic	• 16-bit exponent, 48-bit coefficient in single precision • 16-bit exponent, 96-bit coefficient in double precision
Control Store	64 KBytes
Instruction/Data Cache	32 KBytes
Error Detection	Parity on 8-bit byte basis, all address and data paths, instruction level retry on errors
Number of Independent CPUs	960-11 = 1 960-31 = 1 960-32 = 2
Field Upgrade for Performance	960-11 to 960-31 960-31 to 960-32

Central Memory

Word Size	64 data bits
Number of Banks	8
Bank Access Time	308 nsec
Bank Read/Write Cycle Time	330 nsec
Memory Bandwidth	180 MBytes per second
Error Detection	SECDED on stored data, parity on address and control circuitry
Memory Ports	4
Real Memory Addressing Limit	Up to 2 gigabytes
Capacity	Minimum 64 MBytes, maximum 256 MBytes
Virtual Memory Limits	Up to 8.8 gigabytes per task Up to 4096 segments per task Up to 2147 megabytes per segment

Input/Output Unit

Number of Units	Minimum = 1, maximum = 2
Basic IOU	20 peripheral processors 24 CYBER 170 3-MBytes per second channels
Expansion of Base IOU	5 or 10 DMA I/O processors 5 or 10 DMA I/O channels
Expansion IOU Channels	ISI/DMA Channel, 12 MBytes per second IPI/DMA Channel, 10 MBytes per second 170/DMA Channel, 15 MBytes per second
Peripheral or I/O Processor Memory	16 KBytes per processor
Error Detection/Correction	SECDED
I/O Channel Error Detection	Parity at the byte level or word level for CYBER 170 channel
Remote Maintenance	Yes, via two-port multiplexer
Second IOU Option	Yes

Power	**400 Hz**	**50 Hz**	or	**60 Hz**
Central Processor and Central Memory	13.2kVA	2.8kVA		3.2kVA
IOU(s)	7.9kVA	1.0kVA		1.0kVA

Cooling	**BTU/Hr**
Maximum Heat Rejection Rate	91,000 for base system

Environment

Operating Temperature Range	15°C to 32°C, 60°F to 90°F
Operating Relative Humidity Range	20% to 80%
Dewpoint	24°C, 75°F

Physical Dimensions		**Width**		**Depth**		**Height**	
		cm	**in**	**cm**	**in**	**cm**	**in**
960 Mainframe	Minimum	341.6	134.5	68.6	27.0	193.0	76
	Maximum	445.8	175.5	68.6	27.0	193.0	76
Second IOU	Minimum	106.7	42.0	68.6	27.0	193.0	76
	Maximum	213.4	84.0	68.6	27.0	193.0	76

*Specifications subject to change without notice.

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