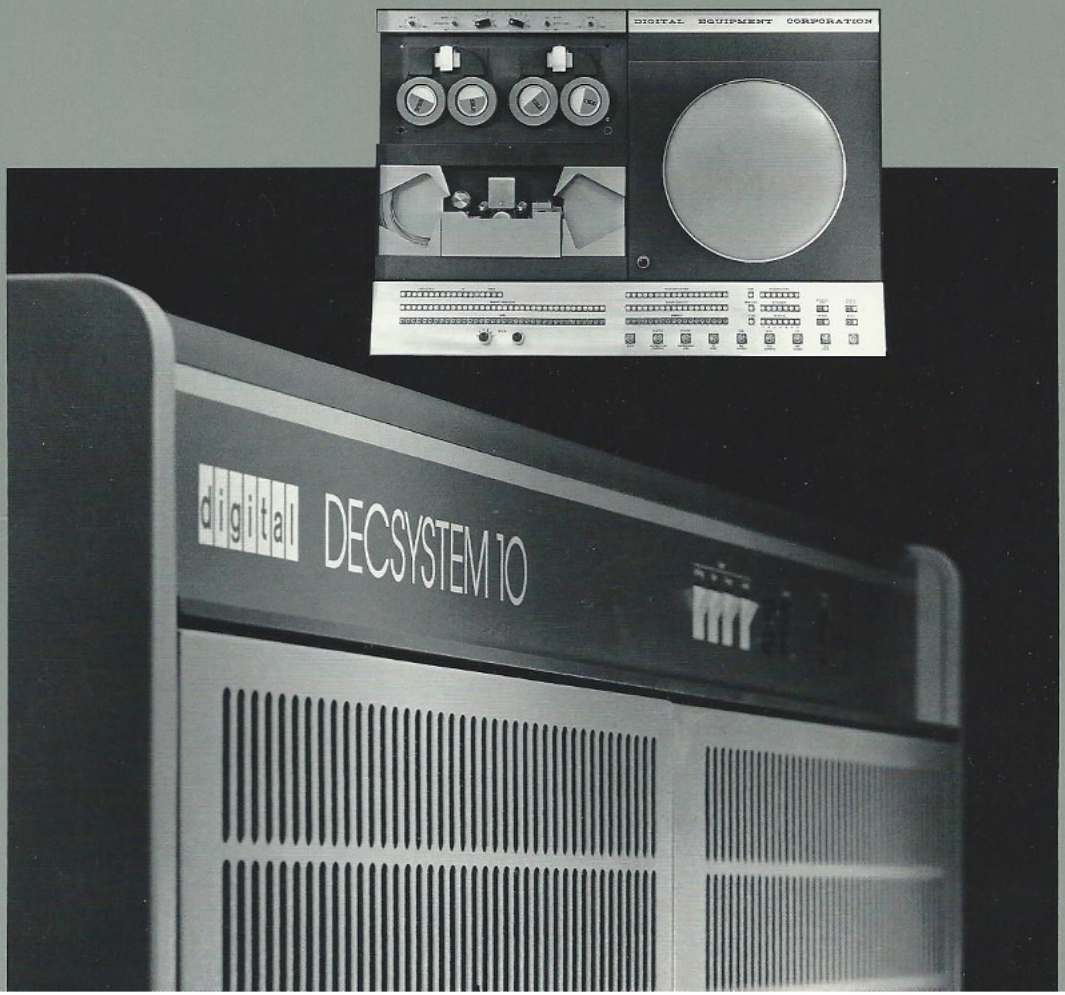
Twenty Years of 36-bit Computing with Digital

digital

1964

1984



This year marks the twentieth anniversary of the first 36-bit computer shipped by Digital Equipment Corporation. Since then, Digital has continued to enhance and develop this important product line.

With this product, Digital was the first computer company to offer commercially available computers for general-purpose timesharing. The first 36-bit products were interactive, easy to use, and, in many ways, ahead of their time. They could be called the "personal mainframes."

The introduction of the 36-bit product line contributed significantly toward making Digital the second-largest computer company in the world.

Digital's 36-bit computers were called general-purpose processors; their uses were limited only by the creativity and technical skill of their users. And among their users were some of the most innovative and sophisticated researchers, scientists, engineers, and business people.

DECsystem-10 and DECSYSTEM-20 computers have been and continue to be leaders in the field of networking. Even before the DECnet era, the TOPS-10 operating system supported ANF, which provided remote stations for terminal concentration, printers, and card readers. Much original ARPANET work was done on TENEX (which evolved into TOPS-20) in the early 1970s. DECnet was supported in TOPS-20 Release 3A in 1978. In early days, more than half of the computers on ARPANET were Digital's 36-bit machines.

The PDP-6 was the first in a product line that inspired loyalty among its users by offering responsiveness, interactive computing, and a way of computing that increased productivity far beyond the output of the card punching of the "other" type of computing.

In addition to timesharing, 36-bit computers provided load balancing, resource sharing, file sharing and reentrant programming, large capacity, and good software. They could be compared with a workshop for the specialist, in that they supplied all necessary tools. The 36-bit products allowed users the freedom to create customized applications and then, if necessary, to change those applications to satisfy other needs.

1964

1984

▸ *The Mill, Maynard, Massachusetts*

▸ *Silicon chip manufacturing at Digital in Hudson, Massachusetts*

▸ 1964

The evolution of the PDP-6, PDP-10, DECsystem-10, and DECSYSTEM-20 series of timesharing computers began in the spring of 1963 and culminated in the delivery of the first commercial PDP-6 in the summer of 1964.

At first, designers of the PDP-6 conceived of the product as a 24-bit system, a logical extension of the Digital line of 12-bit and 18-bit realtime computer systems, but that could provide more performance at an increased price. Several facts changed their thinking.

- 36-bit was the scientific computing standard word length
- IBM mainframes were 36-bit machines
- 36-bits accommodated LISP, the artificial intelligence language developed by Dr. John McCarthy, then at the Massachusetts Institute of Technology.

Considering these facts, the designers decided to make the PDP-6 a 36-bit machine.

The initial design scheme was to provide a powerful, timesharing computer oriented to scientific use. Later, the PDP-6 also was used in commercial environments. The developers of the PDP-6 subscribed to Dr. McCarthy's concept of timesharing, which was to provide each user with the illusion of having his or her own large computer. This was "gentleman's timesharing" – minimal security features, and manual sharing of peripherals and core.

The developers recognized that the machine would have to support a variety of compiled and interpreted languages. Its construction had to be modular so that it could evolve and users could build large systems, including multiprocessors. The

1964

▸ *PDP-6 design team*

▸ *PDP-6*

PDP-6 was designed to be simple, feasible, and supportable by a small organization.

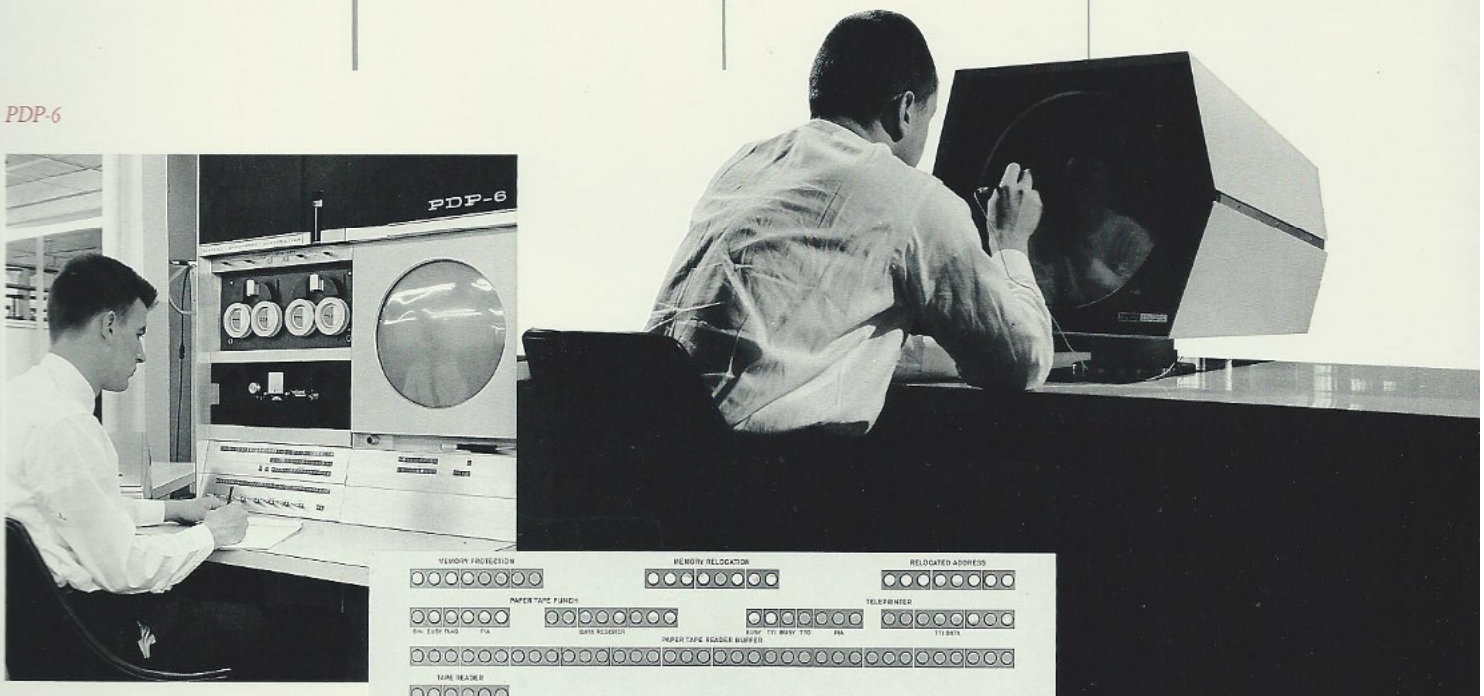
The hardware design team included Gordon Bell, who was the system architect; Alan Kotok, assistant logic designer; Bob Savell, project leader; and Russ Doane, circuit designer. The software design team included Tom Hastings, the first software engineer hired by Digital in 1961; Dave Gross, Tony Wachs, Dit Morse, Harris Hyman, Bill Segal, and Peter Samson. As design and development of the PDP-6 continued, most of the best engineers at Digital participated in bringing the project to completion.

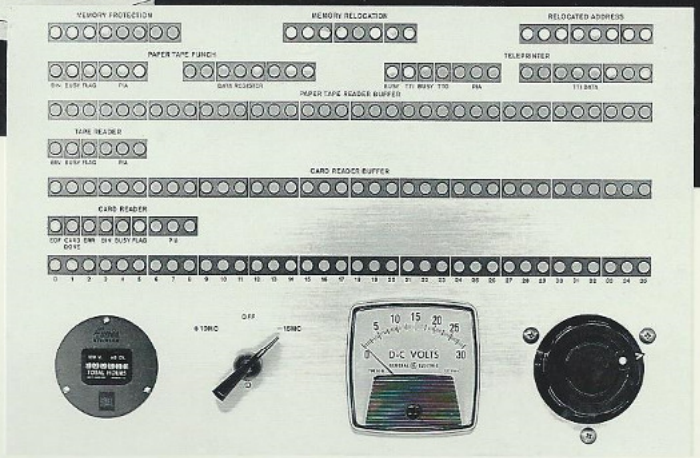
PDP-6 Innovations

PDP-6 influences on the future course of computing include the following:

- It was the *first* machine designed for timesharing. It was powerful enough to support many users, and it was interactive.
- It was the *first* machine to have general-purpose registers. Today, all computers have them.
- It provided general support of stacks in hardware. And the machine had instructions that could process strings of variable size bytes.
- Its 36-bit word was addressable as two 18-bit words. This feature made it suitable for use with LISP.
- Its architecture included a design so innovative that it was patented. Various types of memory and input/output devices could plug into a bus with a standardized protocol, and the bus connected to the central processor. Previously, memory and input/output devices attached directly to the CPU. This was a first for the computer industry and created the opportunity for the add-on industry to begin its development.

▶ *PDP-6*





▶ *PDP-6 maintenance panel*

Some of the initial PDP-6 design decisions defined by Gordon Bell, Alan Kotok, and Tom Hastings included:

- Inexpensive cost per user via timesharing without the inconvenience of batch processing
- Timesharing use via terminals with protection between users
- Direct I/O for realtime users
- Primitive command language
- Modular software to correspond to modular hardware configurations

The PDP-6 System

The system was built of germanium and silicon transistors. Modules were plugged into soldered connectors.

It was massive. The PDP-6 had a 7-track tape drive; card punch, and card reader; line printer; DECtapes, paper tape reader and punch; tabletop Teletype™ 33 terminal. Fast ACs (registers), an option on the PDP-6, fit into a separate 19-inch cabinet.

From 1964 through 1966, the operating systems on the PDP-6 that would evolve into TOPS-10 were Versions 1.4 to 1.9. These versions supported DECtape only, and could handle 27 jobs. The user's manual fit easily on one page.

In total, 23 PDP-6s were built.

PDP-6 Customers and Applications

The first PDP-6 was sold to the University of Western Australia in Perth. Ties between Digital and Australia began when Gordon Bell, then an electrical engineering student at MIT, attended the University of New South Wales as a Fulbright scholar.

▶ *PDP-6s at the Mill in Maynard*

▶ *Alan Kotok*

Later, after joining Digital, Bell hired a former Australian colleague, Ron Smart, to set up and manage Digital's field and sales operation.

At the time that Gordon Bell hired Ron Smart, several people including Gordon Bell and Alan Kotok had already been in Australia working on a proposal to sell PDP-6s to several universities. Ron Smart supported their efforts, and the University of Western Australia acquired the first timesharing machine in Australia.

The PDP-6 was primarily designed for scientific use, and most of its uses were scientific applications. The Stanford Artificial Intelligence Lab, under the direction of Dr. John McCarthy, who had left MIT by this time, was one of its prominent users. The Artificial Intelligence Lab operated a robot car equipped with a television camera using a PDP-6.

Other customers included the Physics Lab at MIT, Brookhaven National Labs, United Aircraft (now United Technologies), and the University of California, Berkeley, where the PDP-6 was used by Dr. Glaser, the inventor of the bubble chamber. Brookhaven National Labs had its PDP-6 constructed in a van so it could be moved from place to place. However, the PDP-6 and van were never moved from their original location.

Some customers used the PDP-6 for timesharing. They were Key Data, Rand Corporation, Applied Logic, and Charles Adams Associates. In Europe, PDP-6 users included the Universities of Bonn, Aachen, and Heidelberg.

1965

▸ *Massachusetts Institute of Technology*

▸ *Brookhaven National Labs van*

Retirement of the PDP-6

In 1965, Win Hindle was asked to become product manager for the PDP-6. He recognized that the PDP-6 was too large and more complex than Digital should have attempted, considering the company's size. He recommended that current orders be filled, but that any further manufacturing of the PDP-6 be stopped.

The PDP-6 designers felt that they could build a new computer based on the PDP-6 that could be quite successful. On their suggestion, Hindle went to the Works Committee with a proposal to start a new computer to be called the PDP-10. Eventually the proposal won approval. Development of the computer that would be called PDP-10 began in mid-1964.

Profiting from its experience with the PDP-6 project, Digital organized the company into "product line" groups. Management could then easily isolate those products that were successful from those that were not and allocate resources accordingly.

1966

▶ *Hand assembly at the Mill, Maynard*

▶ *Win Hindle*

The new central processor was named the KA10.

Alan Kotok, the system architect, headed the PDP-10 hardware design team that included Bob Clements and Dave Gross. The software development team included Tom Hastings, Dave Plummer, Tony Wachs, Valdeane Alusic, Pat White, Nick Pappas, and Alan Frantz.

The PDP-10 was built to work all the time. It was a very solid computer that contributed greatly to Digital's success. PDP-10 architecture varied little from that of the PDP-6, but the PDP-10 ran twice as fast because its electronic circuits were smaller and more robust than those used in the PDP-6.

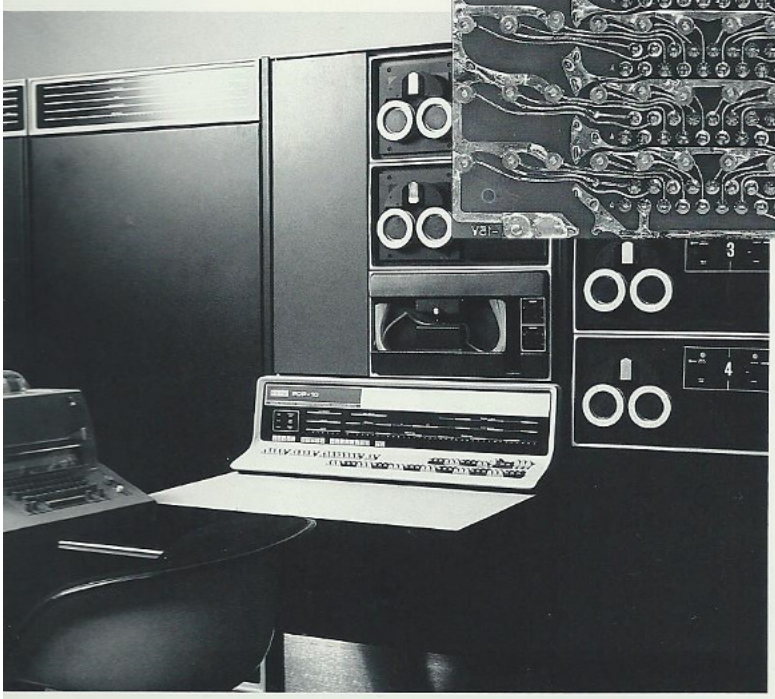
Another reason for the doubled speed was the packaging of the bedsheet boards; there were electrical connections on both ends and in the middle. The PDP-10 was constructed with discrete components. It used Digital's popular Flip Chip modules for logic implementation. Wirewrap technology was used for backplane wiring.

One of the goals of the development project was to offer a smaller, more reasonably priced system with optional features available at additional cost. Another goal was to have a minimum configuration that could be sold for under $100,000. To meet this price, the byte and floating-point instructions were removed from the configuration, it lacked fast ACs, and it had an 8-Kbyte memory. The average configuration cost about $150,000. Totally configured, the system cost $300,000.

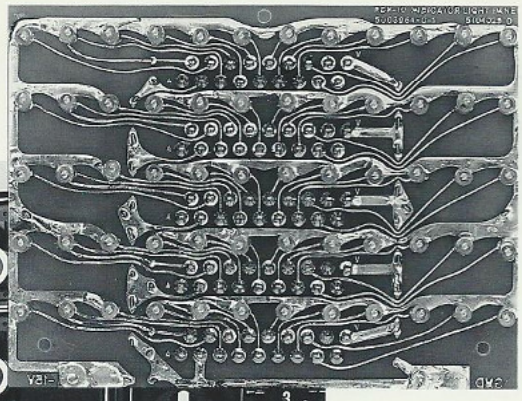
In 1968, TOPS-10 on the PDP-10 supported 36 jobs. By 1969, the operating system could execute about 63 simultaneous independent tasks. In its most popular configuration, it could handle up to 32 concurrent jobs with an average response time to the terminal user of just a few seconds. A typical configuration included 65,536 words of core memory, 500,000 to 1,000,000 words of fast access storage for program swapping, a terminal line scanning unit, a bulk storage disk system, and other appropriate input and output devices.

1967

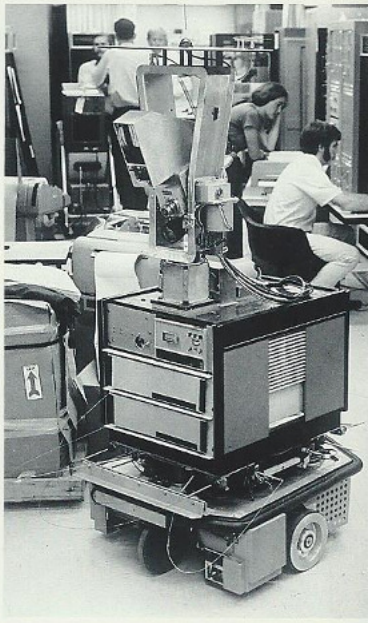
1968



▸ *PDP-10*



▸ *PDP-10 Indicator Light Panel*



▸ *Stanford's robot car*

The PDP-10 software was based upon two upward-compatible versions of the timesharing monitor, a multiprogramming version for totally core resident systems and a multiprogramming swapping version that allowed high-speed, fixed-head storage devices to serve as an extension of core memory. The multiprogramming version accounted for 90 percent of all early sales.

Two Teletype models were regularly available with the PDP-10 for use at the console: the KSR 35, capable of speeds up to 10 characters per second, and the KSR 37, capable of speeds up to 15 characters per second.

The PDP-10 appealed to the same market that had purchased the PDP-6. The PDP-10 was used primarily in university and research and development environments. An important addition was the use of PDP-10s by several large timesharing service utilities.

Between its release in 1967 and 1971, the operating systems that evolved into TOPS-10 supported disk swapping, batch multiprogramming, and monitor support for realtime. The command language and file system were remarkable for their day and their influence can be seen quite clearly on many present-day operating systems for minicomputers and microcomputers, most notably the CP/M® operating system.

▶ 1971

In 1971, the Large Computer Group Special Interest Group (LCG-SIG) was formed, a user group that has proven to be an active participant at DECUS and in interactions with LCG. The original charter reads:

DECUS members interested in the PDP-6 and PDP-10 computers have organized themselves into a PDP-6/-10 Mainframe Committee. It is the purpose of this group of DECUS members to work together within DECUS to improve communication among PDP-6 and PDP-10 users with each other, DECUS and DEC.

At the 1970 fall DECUS Symposium, members representing some thirty PDP-6 and PDP-10 installations voted

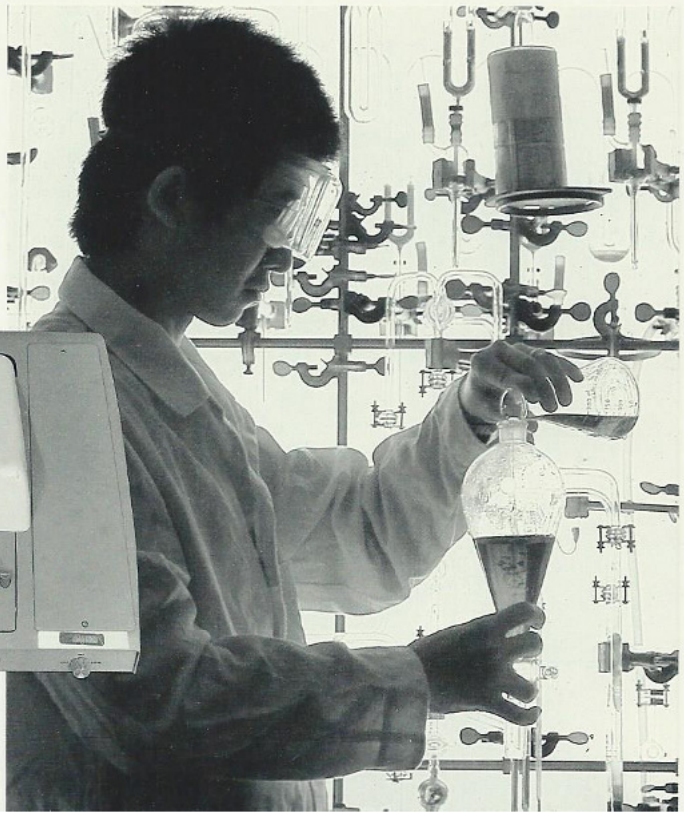
1969

1970

1971

▶ *PDP-10 control panel*

▶ *Teletype™*



unanimously to petition the DECUS Executive Board for official recognition.

Past presidents of LCG-SIG include: George Zepko (Stevens Institute of Technology); William Kropp (Brookhaven National Labs); Eric Knobil (Cornell University); Norbert Kubilus (Rapidata); Paul Treece (Colorado School of Mines); Glen Ricart (National Institute of Health); William Miller (Texas State Purchasing and General Studies); and Leslie Maltz (Stevens Institute of Technology).

▸ 1972

In 1972, the next generation of CPU, the KI10 Central Processor, was first shipped. The KI used TTL logic and introduced "associative memory hardware," which allowed the innovation of virtual memory.

One major change in the computer was the use of integrated circuits. In fact, the I in KI10 stands for integrated circuits. The complete system was named the DECsystem-10.

The architecture was implemented to facilitate memory paging. This allowed memory to be fragmented; in other words, to function as virtual memory. Previously, memory had functioned through protection and relocation, in a contiguous block.

When the first DECsystem-10 multiprocessor system was built in 1972, before the KI10 was announced, Peter Hurley implemented the monitor changes necessary to take advantage of a dual KA-10 configuration with shared memory. This was made possible by the patented memory bus structure of the PDP-6 and PDP-10.

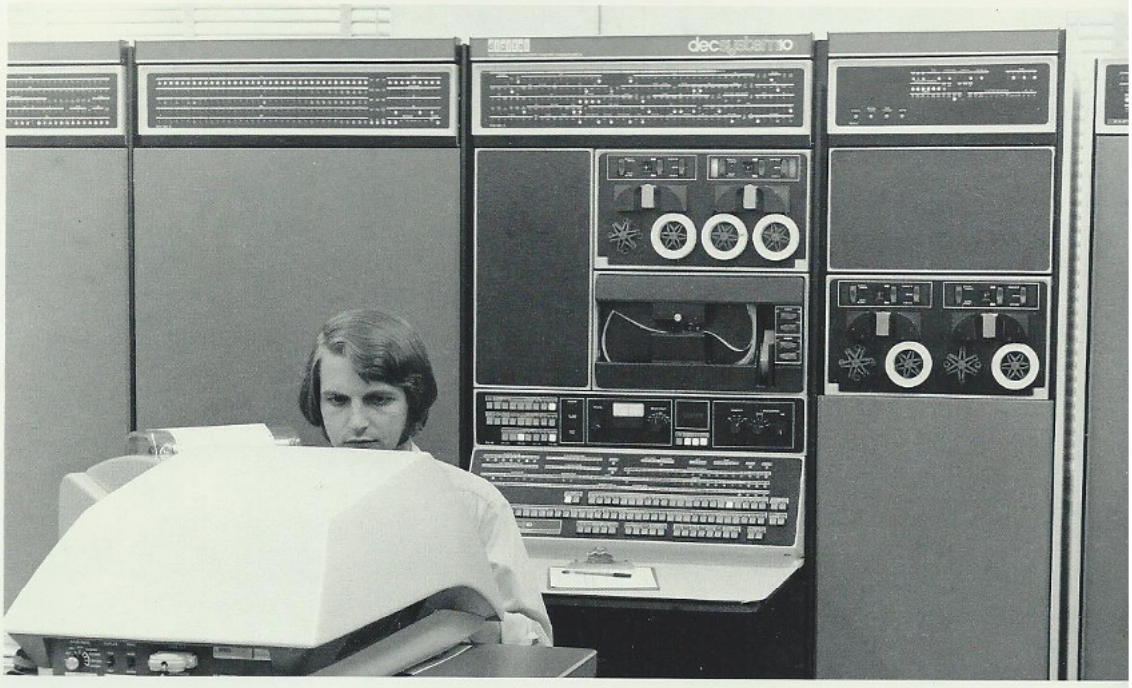
After the completion of the KI10, a new emphasis was placed on developing a low-cost, 36-bit machine. This paved the way for the next generation.

1972

1973

DECUS

▸ *DECsystem-10*



▸ 1976

The subsequent generation of 36-bit central processors was the KL10. Although their primary goal was to produce a low-cost system, the engineers built a faster system. The KL was implemented in ECL (emitter coupled logic). The KI associative memory was expanded, and a sophisticated cache memory design was implemented. The KL is a microprogrammed computer; that is, its instructions are implemented through microcode rather than through "hard wiring." Engineers added a front-end processor and also integrated I/O channels for disks, tapes, and communications into the CPU design. Memory management was made more sophisticated.

During the development of the KL10, some engineers realized that even the "large" 18-bit, 256-Kword address space of the PDP-6/10 architecture would be insufficient in a very few years. This realization resulted in the design of "extended addressing," which was incorporated into the emerging KL10 processor design to extend the addressing capability of the machine to 30 bits, or 8 million words, without invalidating existing programs. Because most

1974 1975 1976

▸ *DECSYSTEM-20*

existing programs could not use extended addressing before undergoing substantial changes, support for including this capability grew slowly over many years.

In 1975, the KL central processor was first shipped running the TOPS-10 operating system, which had supported the KA and KI, as well. In July, the first DECsystem-1080 was installed at a Massachusetts construction company.

Shortly afterwards, the KL was also introduced running the TOPS-20 system. Its marketing designation was DECSYSTEM-20.

The DECSYSTEM-20 supported up to one million bytes of high-speed, low-cost memory. To ensure the reliability of operation and integrity of data, all memory read and write operations were parity checked. The DECSYSTEM-20 featured a large and powerful instruction set and the compilers produced less machine code than comparable systems. Smaller programs ran faster, as well.

The TOPS-20 development team included Dan Murphy, Peter Hurley, Arnold Miller, Len Bosack, Tom Hastings, and Ron McLean. Sue Porada headed the documentation effort, then as now.

In 1972, Digital had bought the rights to TENEX, developed at Bolt Beranek and Newman, by Dan Murphy who came with TENEX to Digital. Members of the development team worked extensively to convert TENEX into TOPS-20. They created disks that would remain readable after a software crash. They redesigned the directory structure. They added search lists, logical names, IPCF, enqueue/dequeue, KL support, wild cards, and pseudo-teletypes.

Much thought was given to the final product name. It began as VIROS, changed to Snark, and was briefly called Krans. Finally, TOPS-20 was selected. Digital announced its first DECSYSTEM-20, available in two versions – the 2040 and 2050.

Digital offered DECSYSTEM-20 as a medium-scale computer with large computer features available at small computer prices. High performance, a virtual memory system that provides a multi-tasking, multiprogramming environment to support concurrent timesharing, batch, and transaction processing were cited as its outstanding features.

▶ *Christian Science Center*

The 36-bit Family

An important design goal for each generation of the 36-bit family (PDP-6, KA, KI, KL) was software compatibility at the assembly language level. Each succeeding family member was capable of running programs – both user and system – from the previous family member. In addition, the central processors themselves were "plug compatible" in that the KL was a "drop-in" replacement for the KA and KI, the KI was a drop-in replacement for the KA, and the KA was a drop-in replacement for the PDP-6.

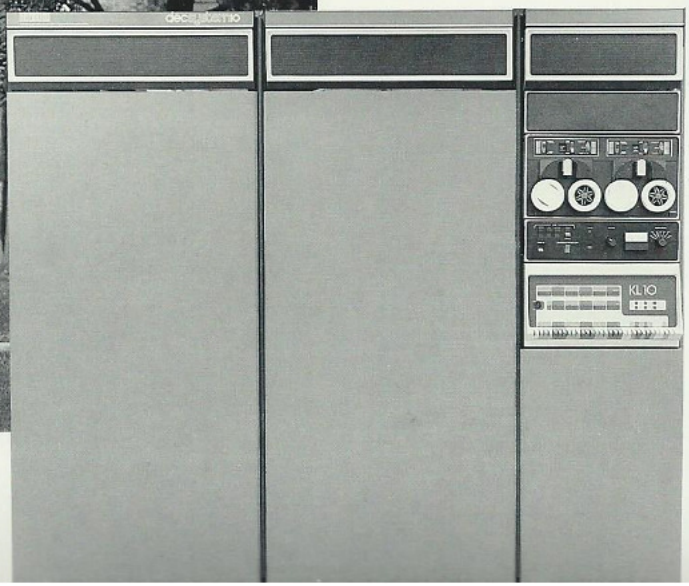
Each successive implementation generally offered increased performance for only slightly increased cost. Allowing for inflation, the KA, KI, and KL cost about the same. However, the KI was almost twice as fast as the KA; the KL two-and-a-half times as fast as the KI, or five times as fast as the KA. So, through 1975 the product design strategy was to produce high-performance processors at about the same cost as the model the new processor replaced, always considering upward compatibility as a constant design goal.

Over 700 of the above systems were installed by January 1978.

DECsystem-10s were vital computing resources to such diverse users as the Stanford Artificial Intelligence Laboratory, U.S. Army Combat Developments Experimentation Command, the Canadian Broadcasting Company, The Christian Science Center, and El Paso County, Colorado Welfare Department. Other customers included the University of Texas Health Science Center, Transportation Systems Center, Cambridge, Massachusetts, and Wilson Synchrotron Laboratory.

DECSYSTEM-20s' customer base includes Union Texas Petroleum, Ford Motors, Stanford University, Abbot Laboratories, R.J. Reynolds and Morgan Guaranty Trust.

1977



▸ *DECsystem-10 with KL10 CPU*

In 1976, the design group set for itself a new goal to build a processor that would provide the capability and speed of the KA at significantly lower cost rather than at the same cost of the preceding processor. Digital attained that goal in producing the KS10 Central Processor.

The development of the 2020 began, and in one year team members had a PDP-10 running the operating system. At that point, they went to the Operations Committee and proposed to build a small PDP-10. The 2020 was the fastest design-to-product project in Digital's history. It cost $250,000 to develop, and was introduced in February 1978. Bob Reid, who had worked on the PDP-6, was the designer.

The KS was introduced as the heart of the new DECSYSTEM-2020 computer system. The announcement stressed that the 2020 was a "real" mainframe computer system – with all of the features of the larger DECSYSTEM-20 models. The KS ran TOPS-20, not a subset of TOPS-20. Language-level programming was just not upward compatible – it was identical. Programs developed on the DECSYSTEM-2040, 2050, or 2060 could be transported to the much less expensive 2020 and run with no modifications. The 2020 extended the range of the DECSYSTEM-20 family and opened important new markets to Digital.

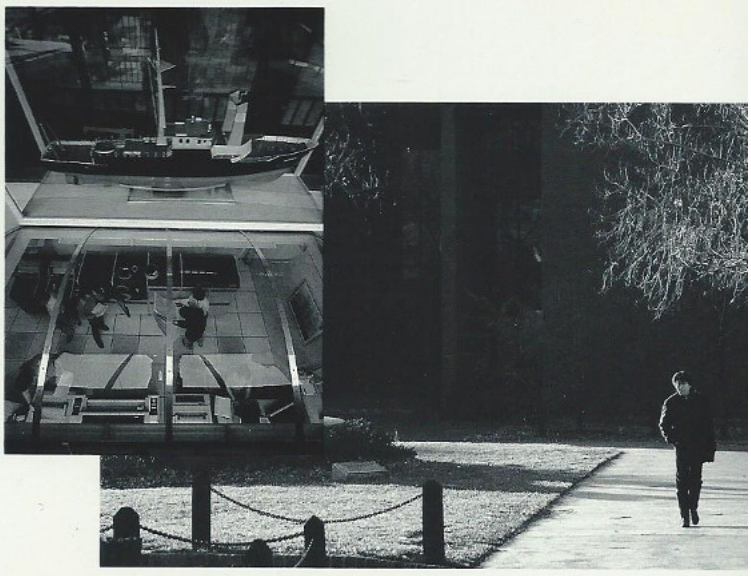
In 1978, Digital recorded sales of $1.4 billion and employed 37,500 people.

1978

1979

▸ *DECSYSTEM-2020*

▸ *Woods Hole Oceanographic Institute*



In 1980, TOPS-10 Version 7.00 was shipped as a controlled release that supported symmetrical multiprocessing, or SMP. SMP was designed primarily for use with a dual DECsystem-1090 configuration using KL10 processors. The SMP capability improved overall system throughput up to 50 percent over traditional master/slave dual-processor DECsystem-10 configurations.

Up to 175 active jobs and up to 512 transaction processing or dedicated-applications terminals could be accommodated. The basic SMP product was software; it was a new version of the TOPS-10 operating system. The hardware remains the same as it is in the master/slave configuration, namely, KL10 hardware with minor enhancements.

SMP software is superior to master/slave software for many reasons. The chief difference is that the I/O devices could now be connected to both CPUs.

Memory is shared between processors and there is still a single copy of TOPS-10. However, the monitor is reentrant and all monitor calls can execute on either CPU.

TOPS-10 7.01 was shipped late in 1980 as a general release. It operated on KS10, KI10, and KL10 single-processor configurations. TOPS-10 DPE (dual-processor extensions) software extended the capabilities of TOPS-10 to dual processor KI10 (DECsystem-1077) and KL10-B/D (DECsystem-1099 A/B) configurations. TOPS-10 DPE updated Version 7.00 and remained optional.

TOPS-20 V4.0 was released and included GALAXY, batch and queueing support; archiving for files; an "execute only" mode for restricting user capabilities; performance controls; and added RAMP features.

Digital, Intel™ and Xerox™ cooperated in the Ethernet local network project that, when complete, set the industry standard for local network communications.

1980

1981

▸ *DECSYSTEM-20*

▸ *Silicon chip manufacturing at Digital in Hudson, Massachusetts*

▸ 1982

DECsystem-1090 TRI-SMP was announced in late 1981, and was first shipped in January 1982 as a controlled release. It provided a significant enhancement to symmetrical multiprocessing (SMP).

Intended for existing single- and dual-1090 sites, TRI-SMP offered a modular growth path for existing SMP installations. TRI-SMP provided the same fully symmetrical multiprocessing capabilities for three processors that the dual SMP provided for two.

These new configurations could support up to 250 active jobs, an increase of 75 jobs from a dual-processor configuration. They were able to handle up to 512 terminals. The addition of the third CPU incurred very little additional overhead and therefore, maximized job handling capability.

The advantages of a TRI-SMP were higher reliability, availability, maintainability and performance, plus less total hardware investment – shared memory, dual-ported disks. It also provided an easy upgrade path, required a smaller operational staff, and allowed access to the entire database by all users. The redundant configuration meant hardware failure resulted in little or no effect except degraded performance.

In 1982, prices for an upgrade option from dual to triple SMP, including hardware and software license, started at $440,000.

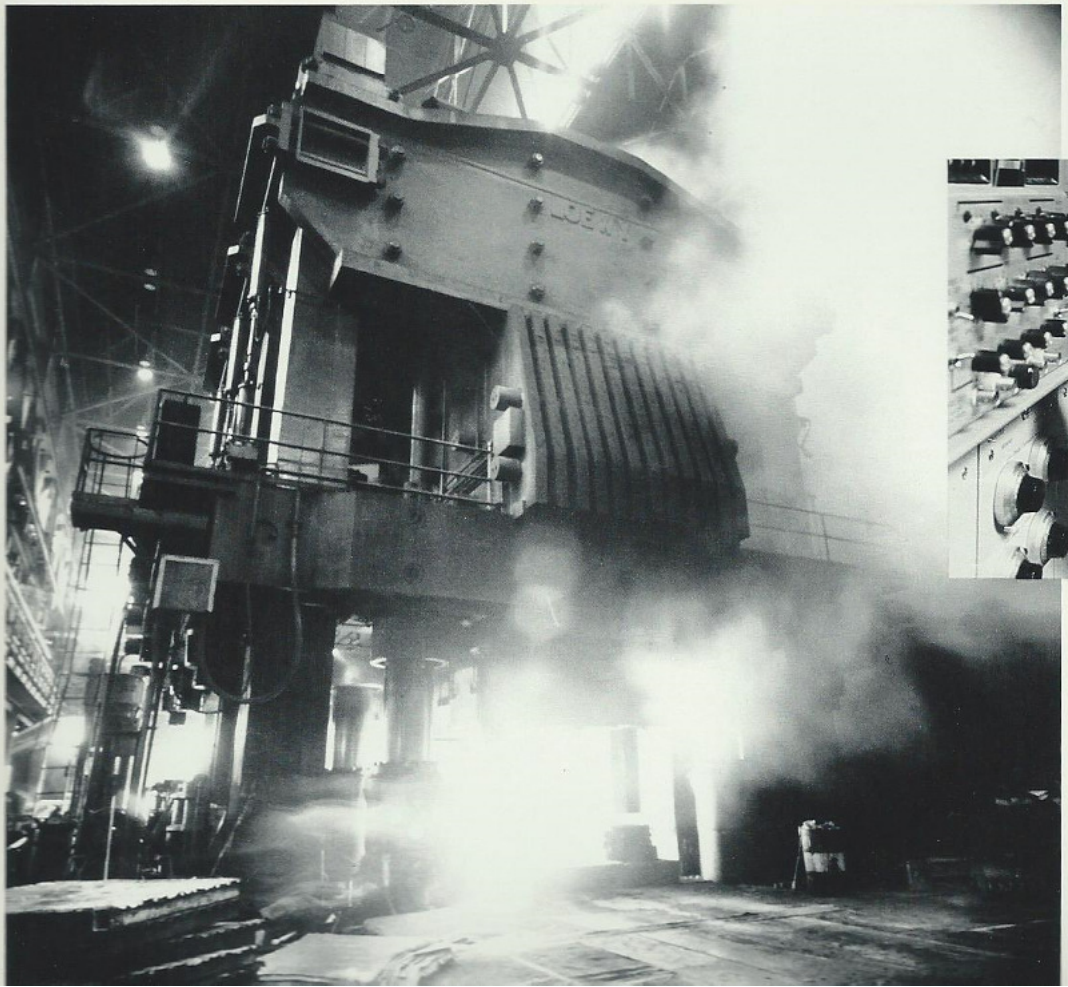
Digital introduced the HSC50 Intelligent Disk/Tape Server designed for multi-host systems. The HSC50 attaches to host processors through standard interconnects and protocols, and supports DSA (Digital Storage Architecture) disk drives and tape formatters. The HSC50 is supported by the DECSYSTEM-20 system, CFS Common File System software, and CI20 hardware.

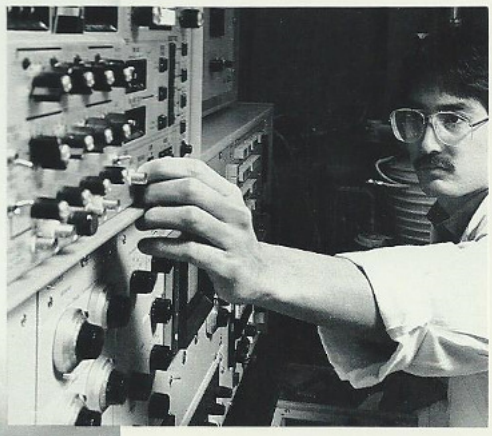
▸ 1983

In 1983, Digital decided to stop development on a planned-for 36-bit machine in order to accelerate incorporation of DECsystem-10 and DECSYSTEM-20 configurations into Digital's other major product architectures. Large Systems immediately formulated a strategy designed to maximize the integration effort for 36-bit installed-base customers. Included in the Integration Strategy was the commitment to continue enhancements on the present DECsystem-10 and DECSYSTEM-20 line for five years, and support the line for ten years, allowing users a substantial amount of time to plan for and incorporate change.

1982

1983





▸ *DECSYSTEM-20 is widely used in manufacturing*

To demonstrate Digital's commitment to the Integration Strategy, major improvements were made to the KL10, which led to the introduction of DECsystem-1095 and DECSYSTEM-2065 within one year. Enhancements to main memory, cache memory, and the pager allow these systems to perform 20 percent better than any previous DECsystem-10 and DECSYSTEM-20.

DATATRIEVE-20, RMS-20, and EDT-20 are introduced. Not only do these software products expand the range of software available to DECSYSTEM-20 customers, they offer command language and other features that are similar to software that is available for other Digital systems.

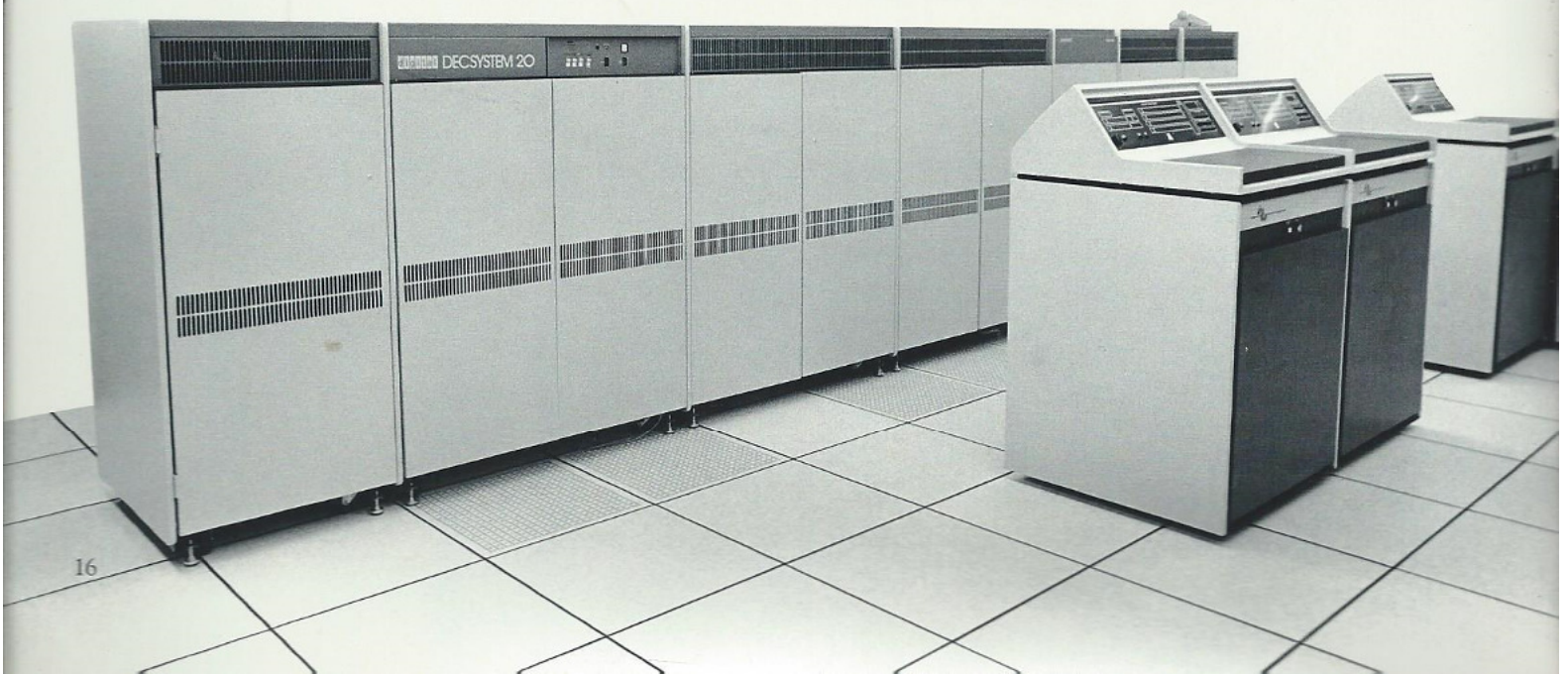
Rose Ann Giordano, vice president of Large Systems Marketing for Digital, says:

"The past 20 years of leadership in developing interactive 36-bit computer systems have helped Digital become the world's second-largest computer company. A key ingredient in these two decades of innovation and success has been our customer – the user. Never has there been a more loyal, dedicated partner in hardware, software, and service development than the PDP-6, DECsystem-10, and DECSYSTEM-20 user base. Digital will continue to support this proud product family as it moves forward, taking advantage of other developing technology to provide users with ever more cost-effective large systems."

1984

▸ *Rose Ann Giordano*

▸ *DECsystem-20*



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