MASSCOMP

The Micro Supercomputer Family

The MASSCOMP 5000 Family of Micro Supercomputers

MASSCOMP's tradition of outstanding price/performance and quality continues with the introduction of new members to our system family. The expanded price/performance range of the 5000 family enables a broader base of users to enjoy performance features normally associated only with supercomputers. MASSCOMP's micro supercomputers are ideal for applications requiring on-site, real-time, and technical computing at an affordable cost.

MASSCOMP provides the customer a wide variety of performance options to balance the system to user needs. The range of options includes floating point accelerators, array processors, data acquisition control processors, graphics subsystems, and high speed networking products.

Typically more expensive superminicomputers do not provide the MASSCOMP 5000 family's range of price/performance and integration.

Architecture

MASSCOMP's 5000 family shares a common system architecture based on MASSCOMP's Triple Bus and RTU, MASSCOMP's real-time enhanced UNIX operating system. Software source compatibility as well as compatibility for Multibus and STD+Bus™ options exist across the Family. Customers may mix-and-match equipment, both from MASSCOMP and other vendors. The Triple Bus design and RTU assure high throughput and balanced performance of system functions. The architecture is the family's foundation.

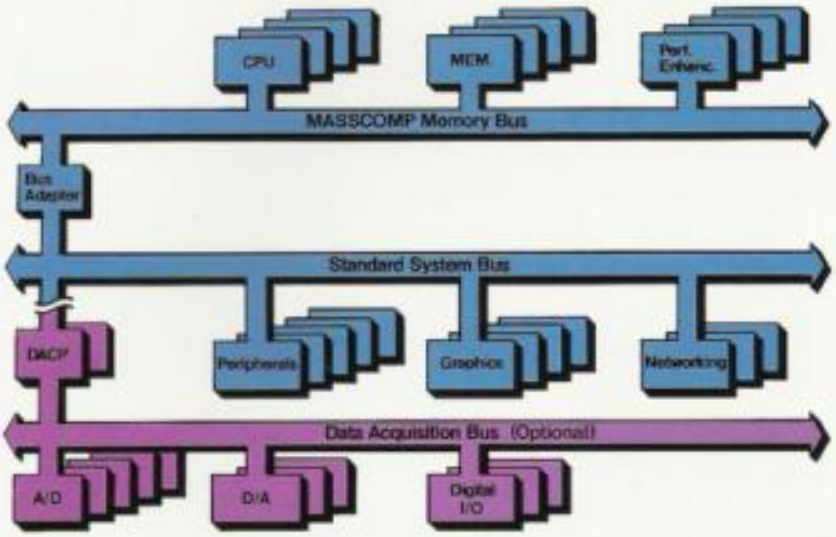
Memory Bus

MASSCOMP's Triple Bus architecture is segmented for maximum performance. The memory bus is the mechanism by which MASSCOMP:

- Optimizes the performance of the systems' computation elements
- Isolates the most rapidly changing segment of technology from customer investments in system peripherals and software

Attached to this bus are the CPU, memory, performance enhancements (for example FPP, AP), and bus adapter.

System memory connects to the memory bus to ensure an efficient data path with the CPU. Together with MASSCOMP's memory management and cache implementation, high-speed data transfers eliminate bottlenecks found in many single bus architectures, ensuring optimum compute performance.



MASSCOMP's Triple Bus Architecture