The PowerPC 603e microprocessor is a low-power implementation of the PowerPC™ Reduced Instruction Set Computer (RISC) architecture. The PowerPC 603e microprocessor offers workstation-level performance packed into a low-power, low-cost design ideal for desktop computers, notebooks, and battery-powered systems.

Superscalar Microprocessor
The PowerPC 603e microprocessor design is superscalar, capable of issuing three instructions per clock cycle into five independent execution units:
- Integer unit
- Floating-point unit
- Branch processing unit
- Load/store unit
- System register unit

The ability to execute multiple instructions in parallel, to pipeline instructions, and the use of simple instructions with rapid execution times yields maximum efficiency and throughput for PowerPC 603e systems.

Power Management
The PowerPC 603e microprocessor features a low-power 3.3-volt design with three power-saving modes—doze, nap and sleep. These user-programmable modes progressively reduce the power drawn by the processor.

The PowerPC 603e microprocessor also uses dynamic power management to selectively activate functional units as they are needed by the executing instructions. Unused functional units enter a low-power state automatically without affecting performance, software execution, or external hardware.

Cache and MMU Support
The PowerPC 603e microprocessor has separate 16-Kbyte, physically-addressed instruction and data caches. Both caches are four-way set-associative.

The PowerPC 603e microprocessor also contains separate memory management units (MMUs) for instructions and data. The MMUs support 4 Petabytes (2^50) of virtual memory and 4 Gigabytes (2^32) of physical memory. Access privileges and memory protection are controlled on block or page granularities. Large, 64-entry translation lookaside buffers (TLBs) provide efficient physical address translation and support for demand virtual-memory management on both page- and variable-sized blocks.

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Flexible Bus Interface

The PowerPC 603e microprocessor has a selectable 32- or 64-bit data bus and a 32-bit address bus. Support is included for burst, split and pipelined transactions. The interface provides snooping for data cache coherency. The PowerPC 603e microprocessor maintains MEI coherency protocol in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

PowerPC 603e Microprocessor Major Features

Specifications
- 16-Kbyte instruction and 16-Kbyte data caches
- Superscalar—3 instructions per clock cycle
- On-chip power management
- 32/64-bit data bus mode
- Fully JTAG-compliant

Performance

\[ 100 \text{ MHz} \]

- SPECint92* 120
- SPECfp92* 105

Power Consumption

- Full operation—3.5 watts maximum at 100 MHz
- Low Power Modes—doze, nap, sleep

Technology

- 3.3-volt implementation
- 0.5-micron static CMOS technology
- 98 mm\(^2\) die size
- 2.6 million transistors

Packaging

- 240 CQFP/256 BGA

*Estimated performance.

For additional information, call
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