



Model 3230

The Model 3230 is Perkin-Elmer's midrange system offering in the Series 3200 family of Megamini® computer systems. This versatile, high performance machine is expandable to 8 megabytes of directly addressable main memory, allowing parallel development of large complex programs without cumbersome paging techniques. As a member of the Series 3200 family, it is program compatible with the other Series 3200 processors.

In keeping with Perkin-Elmer's proven reputation for producing the most reliable minicomputer systems available, the Model 3230 incorporates more than a decade of innovative design and technological leadership. New standards have been established that are designed to provide high reliability, maintainability, and ease of use while expanding previous limits for processing power, system capacity, integrity and accuracy.

PRODUCT DESCRIPTION

Central Processor Unit

The Model 3230, as shown in Figure 1, is designed for applications which require the power and flexibility of a 32-bit architecture balanced by cost/performance constraints. The characteristics and features of this system include:

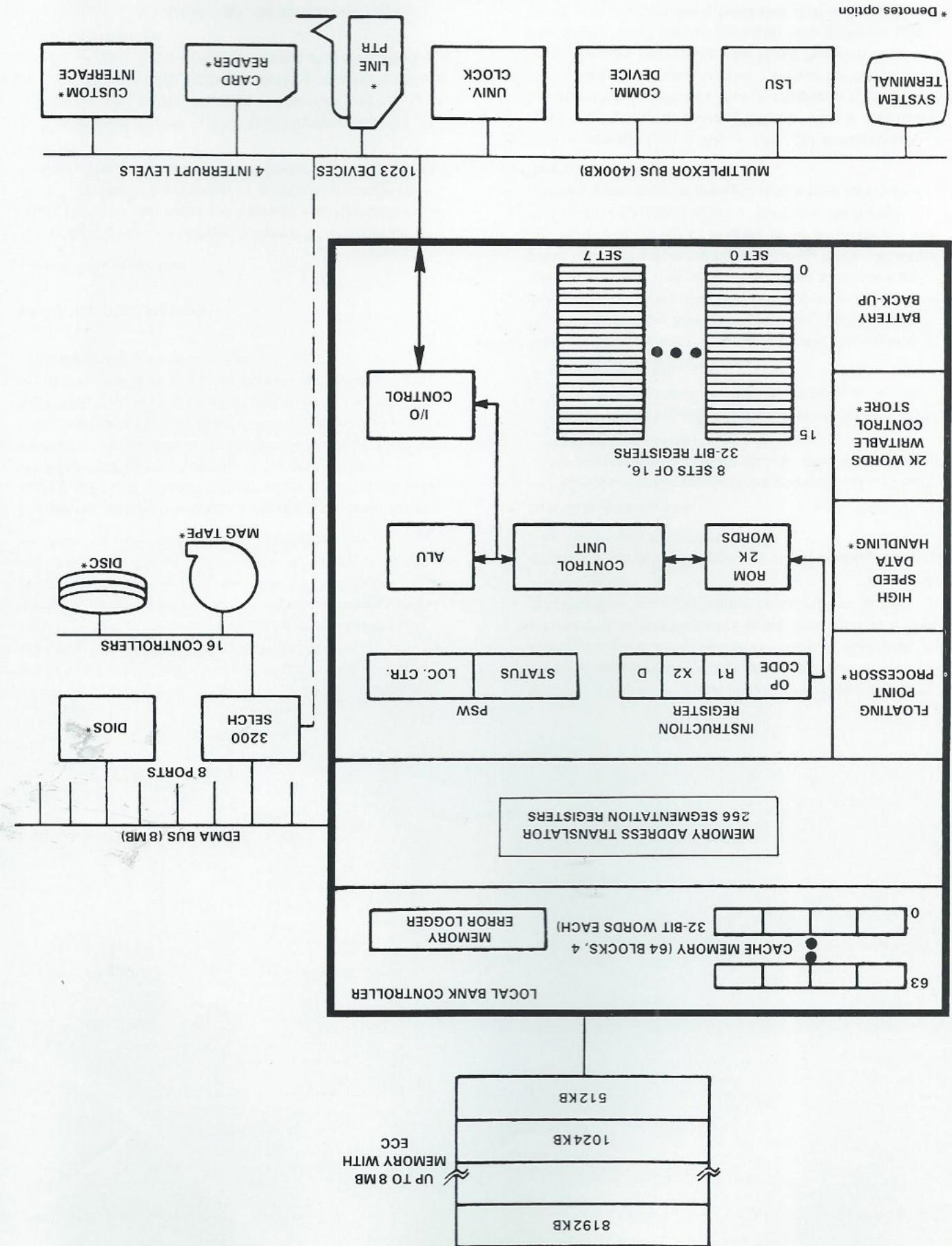
- 32-Bit Architecture — The 3230 incorporates 32-bit internal data paths, allowing for parallel processing of data. The memory modules, general-purpose registers, and writable/fixed control store are also formatted in a 32-bit structure.
- Registers — A total of 128, 32-bit general registers (eight sets of 16) are provided as a standard feature. They include four dedicated register sets for handling

the four external interrupt levels. The remaining four sets are allocated by the operating system as necessary. Multiple register sets obviate the need to save and restore the general registers every time there is a context switch, thus significantly reducing the context switch times.

- Interrupt Support — Support of 1023 unique devices on four independent interrupt levels.
- Dual Bus Architecture
 - High-speed machine/machine communications path for interfacing secondary storage devices such as disc and tape units.
 - Medium-speed man/machine communications path for interfacing devices such as printers, consoles, card readers, etc.
- Memory Management — Integral to the processor is a Hardware Memory Manager which provides memory segmentation, relocation and protection under operating system control. This device translates a program address into a physical memory address. It also monitors all memory accesses to provide write and execute protection of a specified block of memory. Hardware memory management ensures that a task exists in a fully protected environment.
- Loader Storage Unit (LSU) — The LSU automatically loads the Operating System, OS/32, from a secondary storage device such as a disc or magnetic tape. This load operation can occur after a power fail sequence, or upon operator intervention for Initial Program Load (IPL). The Series 3200 bootstrap loader also performs additional memory/processor tests before the Operating System is loaded, further assuring the user of a fully operational system.

Figure 1. 3230 Block Diagram

* Denotes option



- **Integrated System Console** — A 550 VDU that facilitates easy control and monitoring of the system's status with easily understandable messages.
- **System Control Panel** — A consolette is provided as a system control/monitor panel. The consolette has four control switches for HALT/RUN, SINGLE STEP, IPL ENABLE/DISABLE, and IPL INITIALIZE. Four LED indicators display CPU Power Ready, Wait, Fault, and System Power Fail. Finally, the consolette also has a power standby/on/lock key switch.
- **Universal Clock** — Includes a programmable precision interval clock and an AC line frequency derived clock.
- **Two Line Communications Multiplexor** — Provides two, asynchronous communications lines, one of which is used for the system console. The other is available with data rates of 150, 600, 4800, or 9600 baud, RS232C or current loop.
- **Cache Memory** — The 3230 is configured with a 1KB, direct-mapped cache, organized into 64 blocks, each 16 bytes long. Cache consists of a high-speed bi-polar memory residing between the processor and the memory system and provides a significant performance enhancement. Cache implementation reduces the effective access time of main memory from 500ns to 340ns, based upon an 80% cache hit ratio.

Whenever the processor tries to read from main memory, it first checks if the data already exists in the cache. If so, the processor reads from the high-speed cache memory, rather than main memory. An 80% hit ratio is typical, meaning that 80% of the times data is available from the high-speed cache memory.

The actual hit ratio depends upon how the user programs and data are organized; the performance improvement typically ranges from 10-25% with an average hit ratio of 80%.

Optional features for the 3230 include:

- **Floating Point Processor (FPP)** — The high-performance Floating Point Processor option provides 48 single and double-precision floating point instructions. It also contains eight 32-bit single-precision registers and eight 64-bit double-precision registers. Twelve instructions are available to transfer data between the single and double-precision registers for mixed-mode calculations. High floating point accuracy is achieved via R-Star rounding. This rounding technique, implemented in the Series 3200 provides more accurate results over extended calculations, as opposed to conventional rounding.
- **Data Handling Option** — The Data Handling option is primarily used for data communications applications, and provides fast, more efficient operation. Two instructions, Process Byte and Process Byte Register, are used to calculate a cumulative checksum based on an old checksum and a new data byte. The check can be used for BISYNC or SDLC.
- **Writable Control Store (WCS)** — Writable Control Store offers 2048, 32-bit words of user-alterable control storage for custom-tailoring the Model 3230 to a

specific application. Special scientific or mathematical algorithms, communications protocols, or time-critical subroutines can be easily implemented in WCS. The microprogrammed routines typically execute two to three times faster than the equivalent assembly level routines. WCS is supported by appropriate microcode development software.

MEMORY SYSTEM

The Model 3230 supports up to 8 megabytes of memory. Using 16K dynamic RAM chips, memory is composed of 512KB modules achieving an access time of 500ns. The 3230 is available in two memory expansion configurations; one to a 4MB/unit, and one to an 8MB/unit. The memory system can be expanded in 512KB increments, to the full complement of either 4MB or 8MB.

Error Correcting Code (ECC)

Error correction is standard with the 3230 memory system. A seven-bit code is appended to each 32-bit word which allows correction of all single bit errors, and detection of many multiple bit errors. ECC significantly improves the reliability and confidence level of the memory system.

Error Logger

The Error Logger records data that identifies error trends. The collected data serves a twofold purpose. First, it is used to isolate faulty memory chips before they affect memory system reliability and secondly, to isolate other types of system malfunctions.

Battery Back-Up

Since MOS memory is volatile, the Model 3230 includes a battery power retention system. It provides power to maintain the contents of the memory, based on the configuration, for up to 53 minutes. When line power is lost, the battery system automatically provides the power to retain memory contents. This includes the processor state, which is stored in main memory when a power fail is detected. Upon restoration, the processor reloads its registers and resumes operation.

I/O ARCHITECTURE

The 3230 incorporates two external communications busses. The man/machine interface, referred to as the multiplexor (MUX) bus, interfaces medium speed devices such as printers, consoles, card readers, etc.

The machine/machine path, referred to as the Enhanced Direct Memory Access (EDMA) bus, interfaces secondary storage devices such as discs and mag tapes. Thus, the I/O architecture can be optimized to specific application needs.

Multiplexor Bus

The multiplexor bus supports up to 1023 devices, divided among the four interrupt levels. Each level has a unique register set associated with it to speed context switching between levels.

Data transfers over the multiplexor bus are accomplished in two ways:

- (1) A byte or halfword transferred between a multiplexor bus device and memory, under control of an I/O instruction.
- (2) Multiplexed blocks of data transferred between a multiplexor bus device and the memory. This is accomplished by the Auto Driver Channel, which is driven by the fixed control store. The channel performs automatic character translation and computes CRC/LRC values used in communications devices. These devices use the Auto Driver Channel because it offers faster, more efficient operation than the comparable assembly-level instruction sequence.

EDMA Bus

The EDMA bus supports eight high-speed ports directly to and from memory. Each port is controlled by a selector channel, which initiates and terminates data transfers. The selector channel is programmed using the multiplexor bus; once the channel is activated, the processor is free to continue processing.

Each selector channel can, in turn, support 16 device controllers and transfers burst groups of 8 halfwords to or from the memory.

Under burst mode, the selector channel can transfer 5.71MB/sec when writing to memory, and 8MB/sec when reading from memory. A special UDMAI logic interface is also available for implementing custom-designed interfaces.

DIOS

The DMA I/O Subsystem (DIOS) is a high performance, Intelligent Communications Controller for the Series 3200. The DIOS provides DMA facilities between main memory and multiple I/O devices, thus allowing data transfers to take place with no processor intervention. System throughput is therefore dramatically improved.

The DIOS can support up to 63 two-wire or 31 four-wire data communications devices.

Reliability/Maintainability

The Model 3230 is designed to be the most reliable minicomputer system available. Features that provide reliability and maintainability have been designed into all aspects of component production and continue with one of the most extensive system testing procedures in the industry. These features include:

- Error Checking and Correcting (ECC) — The ECC feature will detect and correct all single bit errors and detect multiple bit errors.
- Error Logger — A journal of all errors that have been detected by the ECC feature. The contents of the Error Logger can be examined at any time in the form of a report. Suspected problems in memory can be repaired during scheduled preventative maintenance periods, eliminating costly downtime.

- Battery Backup — Provides memory integrity in case of power failures or brownouts for a period of 53 megabyte minutes.
- Self Test — When power is applied to the system, the basic memory and processor functions are checked. Additional memory and processor checks are performed when the operating system is loaded.
- Diagnostics — Multimedia diagnostic programs for the processor, memory and all peripherals are available with the purchase of the operating system.
- Remote Diagnostics — Provides the ability to remotely demonstrate a hardware problem to a highly trained support engineer located in one of Perkin-Elmer's nationwide service centers. The Remote Center can completely exercise and diagnose the system.
- Power Fail/Auto Restart (PF/AR) — Provides system integrity in case of power failure. Upon power restoration, the processor will restore its' environment and resume operation.
- Illegal Instruction Trap — All floating point, WCS and high-speed data handling instructions are treated as illegal instructions if the appropriate option is not in the system, thus preventing a system failure.
- Power System — Modular power subsystem with extensive maintenance features.
- System Testing — All systems must pass an extensive series of operational and environmental tests before shipment.

INSTRUCTIONS

The Series 3200 instruction set includes a comprehensive array of instructions for general-purpose processing in Simulation, Scientific, Seismic, CAD/CAM, Data Communications, and Commercial applications as well as other general applications. The instruction set performs the following classes of operations:

- Load/store halfwords, fullwords and multiple words
- Fixed-point arithmetic on halfwords and fullwords
- Logical operations (AND, OR, exclusive OR, Compare and Test) on the halfwords and fullwords
- Logical and arithmetic shifts and circular rotation of halfwords and fullwords
- Extensive bit manipulation
- Floating-point arithmetic on single (32-bit) and double (64-bit) precision operands
- List operations
- Data handling operations
- Input/output
- Byte manipulations
- Writable Control Store operations
- Mixed-mode floating point arithmetic
- Privileged system functions
- Storage-to-storage functions
- Decimal conversion

The Series 3200 instruction set uses the eight different instruction formats illustrated in Figure 2.

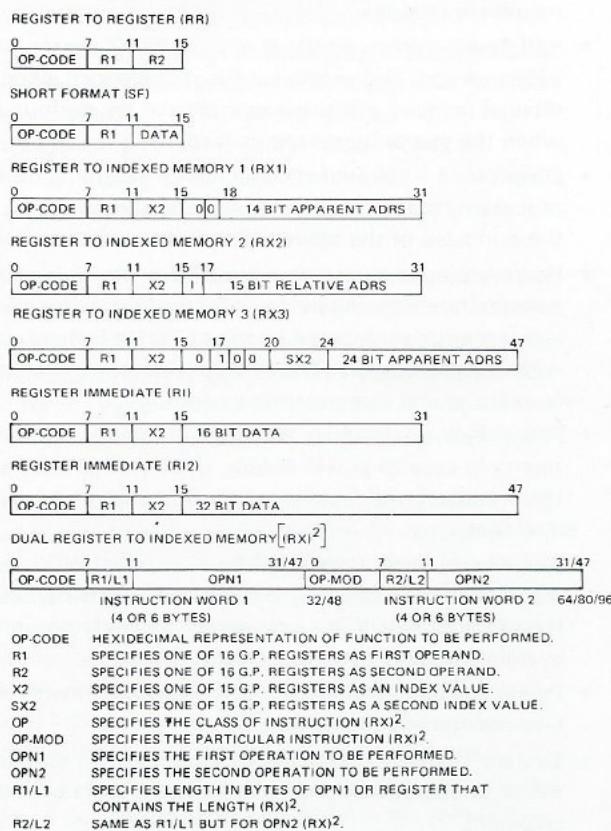


Figure 2. Series 3200 Instruction Formats

CONFIGURATION

The basic 3230 system consists of:

- 512KB of MOS Memory with ECC
- Error Logger
- 1KB Cache Memory
- Memory Management Hardware
- 53 Minute Battery Backup (1MB)
- 8 sets of 16, 32-bit general registers
- Loader Storage Unit with Bootloader
- Universal Clock
- Power Fail/Auto Restart
- Model 550VDU as a System Console
- 2 Line Communications Multiplexor
- 3200 SELCH
- 17-Slot CPU Chassis
- 8-Slot I/O Chassis
- 150 Amp Power Supply
- 56" beige cabinet with AC distribution panel
- System Control Panel

COMPATABILITY

The Model 3230 is user software compatible with all Series 3200 processors. All Perkin-Elmer 32-bit processors run under the standard OS/32 operating systems, and all high level languages are totally compatible across the entire Series 3200 product line.

The multiplexor bus on the 3230 is compatible with all Series 3200 systems. 3240, 3220, 8/32 or 7/32 DMA devices may be used on the 3230, provided a 3200 Selector Channel is provided.

Microprograms developed using Model 3220 or Model 3240 microcode format will need modification before being used on the 3230.

SPECIFICATIONS

Technology

Processor	Schottky TTL, MSI, LSI
Control Store	70ns bipolar ROM
WCS	60ns High Speed Static RAM
Main Memory	150ns, 16K Dynamic RAM
Cache Memory	45ns, bipolar RAM

Processor

General Registers	8 sets of 16, 32-bit general registers
Floating Point Registers	8, 32-bit single-precision floating point registers 8, 64-bit double-precision floating point registers
User Instructions	200 instructions including 48 floating point, 2 data handling, 6 commercial, 4 WCS instructions
Addressing	Direct to 8MB Relative to \pm 32KB Single and double indexing to 8MB Absolute to 16MB
Arithmetic	2's complement

Memory

Main Memory	MOS
Type	150ns access time, 16K Dynamic RAM
Data Length/Access	16, 32, 64, or 128 bits
Data Paths	32-bits
Size	Up to 8MB using 512KB modules
Access Time	340ns effective, with cache 500ns without cache

Cache Memory

Size	1KB
Organization	64 blocks, each 16 bytes long
	Direct mapped Write-Through

I/O

Max. number of devices	1023
Priority	4 interrupt levels Daisy chain priority on each level
EDMA bus ports	8
EDMA transfer rate using 3200 selector channel	8MB/Sec in Burst Read Mode (8Halfword bursts) 5.71 MB/Sec in Burst Write Mode (8Halfword bursts)

Environmental

Temperature	0-50 °C
Humidity	50-90% (noncondensing)
Vibration	0-55HZ at 1.25G's
Storage Temperature	-55 °C to 85 °C
Power Requirements	180-264 VRMS (brown-out protection), 47-63Hz, 20.0 amps maximum

PRODUCT NUMBERS

M32-202	Model 3230 with 512KB Memory, expandable to 4MB
M32-203	Model 3230 with 1MB Memory, expandable to 4MB
M32-204	Model 3230 with 2MB Memory, expandable to 4MB
M32-205	Model 3230 with 1MB expandable to 8MB
M32-206	Model 3230 with 2MB expandable to 8MB
M32-100	Memory Expansion, $\frac{1}{2}$ MB
M32-101	Memory Expansion, 1MB
M32-011	2K WCS on 800 cpi Magnetic Tape
M32-016	2K WCS on 1600 cpi Magnetic Tape
M32-017	2K WCS on 10MB disc
M32-004	Floating Point Processor
M32-005	High-Speed Data Handling

RELATED DOCUMENTATION

47-004	Model 3230 Installation and Maintenance Manual
29-721	Model 3230 Users' Manual
47-005	Model 3230 Micro Programmer's Reference Manual

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Manufacturing facilities, and Sales/Service offices throughout the world.

The information contained herein is intended to be a general description and is subject to change with product enhancement.

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